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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,838	11/26/2003	Suan Jeung Boon	303.601US3	8165

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MINNEAPOLIS, MN 55402

EXAMINER
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MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
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2813

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/722,838	<b>Applicant(s)</b> BOON, SUAN JEUNG	
	<b>Examiner</b> James M. Mitchell	<b>Art Unit</b> 2813	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 26 December 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-9, 27-33 and 59-66 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 27-33 and 59-66 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/26/06</u> . | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is in response to applicant's amendment filed December 26, 2006.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1, 27, 28 and 30-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al. (U.S. 6,245,595).
4. Nguyen (Fig. 3, 5, 6) discloses:  
  
(cl. 1) a method of packaging comprising: applying an adhesive (214) to a first side of a finished wafer (100), the first side of the finished having at least one die (102), the adhesive being one or more of an elastomer (e.g. "silicone" material is compliant-rubber like material) applied in fluid form ("inject"; step 610; Fig. 6), a thermoplastic material, or a pressure-sensitive film (Col. 6, Lines 14-21); and forming an array of conductive elements (108) within the adhesive to a level to allow the adhesive to contact a support (502) to attach the at least one die to the support (Col. 6, Lines 45-49), the array of conductive elements electrically coupled to an array of connection pads (104) on the at least one die;

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(cl. 27) forming an array of conductive elements (108) within an adhesive layer; and applying the adhesive layer to a first side of a finished wafer, the first side of the finished wafer having one or more dice<sup>1</sup> (102), after forming the array of conductive elements to couple the array of conductive elements electrically to an array of connection pads (104) on a first die of the one or more dice (Fig. 3);

(cl. 28) wherein forming an array of conductive elements within an adhesive layer includes forming openings in the adhesive layer (e.g. space taken by conductive elements forms openings);

(cl. 30) an array of conductive elements includes forming an array of solder columns (108; Col. 5, Lines 5-6; Fig. 5);

(cl. 31) an array of conductive elements includes forming an array of solder balls (Fig. 3);

(cl. 32) applying the adhesive as a thin coating (Fig. 4) and therefore a film;

(cl. 33) singulating the first die (step 614; Fig. 6) from the coated wafer and forming an individual flip chip (e.g. contacts 108 near active area; Fig. 5).

5. Claim 1, 27, 28 and 30 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. (U.S. 6,528,349).

6. Patel (e.g. Fig. 2H, 2I, 4A, 4B) discloses:

(cl. 1) a method of packaging comprising: applying an adhesive (14) to a first side of a finished wafer (11), the first side of the finished having at least one die (Col. 3, Line 39-

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<sup>1</sup> Understood from the elected species to mean an IC formed on the wafer.

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42), the adhesive being one or more of an elastomer (compliant polymer; Col. 4, Lines 9-11) applied in fluid form (e.g. "spray"; Col. 4, Lines 13-19), a thermoplastic material, or a pressure-sensitive film; and forming an array of conductive elements (16) within the adhesive to a level to allow the adhesive to contact a support (e.g. portions of adhesive material in contact with support; Fig. 4B) to attach the at least one die to the support (Col. 3, Lines 33-36), the array of conductive elements electrically coupled to an array of connection pads (12) on the at least one die (by layer 20);

(cl. 27) forming an array of conductive elements (16) within an adhesive layer; and applying the adhesive layer to a first side of a finished wafer, the first side of the finished wafer having one or more dice (e.g. IC connected to die pad), after forming the array of conductive elements to couple the array of conductive elements electrically to an array of connection pads (12) on a first die of the one or more dice (by layer, 20; Fig. 4B);

(cl. 28) wherein forming an array of conductive elements within an adhesive layer includes forming openings (27) in the adhesive layer;

(cl. 30) an array of conductive elements includes forming an array of solder columns (16; Col. 5, Lines 34-35);

(cl. 32) applying the adhesive as a thin coating (Fig. 4B) and therefore a film.

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-4, 6-9, 27- 33, 59, 60, 62, 63, 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen'881 et al. (U.S. 6,352,881) in combination with Nguyen'595 (U.S. 6,245,595).

9. Nguyen<sup>2</sup> (e.g. Fig. 3a-c, 4) discloses:

(cl. 1, 59) a method of packaging comprising: applying an adhesive (214) to a first side of a finished wafer (100), the first side of the finished having at least one die (102), the adhesive being one or more of an elastomer (e.g. "silicone" material is compliant-rubber like material; CLAIM 5 of Nguyen'881); a thermoplastic material, or a pressure-sensitive film (Col. 6, Lines 14-21); and forming an array of conductive elements (306) within the adhesive to a level to allow the adhesive to contact a support (Fig. 1g) to attach the at least one die to the support (Fig. 1g), the array of conductive elements electrically coupled to an array of connection pads (104) on the at least one die;

(cl. 2, 4, 28, cont. cl. 59) wherein forming an array of conductive elements within an adhesive layer includes forming/processing openings in the adhesive layer (302) aligned with connection pads (104);

(cl. 3, 9) the method performed in the order presented (Fig. 4);

(cl. 6, 33, 63) singulating the first die (step 410; Fig. 4) from the coated wafer and forming an individual flip chip (Fig. 1g);

(cl. 7) mounting the chip to a receiving support (114);

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<sup>2</sup> Note Ohuchi's Figure 6 also could have been used to anticipate the claimed invention in a similar manner and make obvious use of a fluid to form an adhesive on a wafer.

(cl. 8) curing adhesive (e.g. step 412; Fig. 4);

(cl. 27) forming an array of conductive elements (306) within an adhesive layer; and applying the adhesive layer to a first side of a finished wafer, the first side of the finished wafer having one or more dice (102), after forming the array of conductive elements to couple the array of conductive elements electrically to an array of connection pads (104) on a first die of the one or more dice (Fig. 3b);

(cl. 29) the openings formed by laser cutting, chemical etching or die cutting (Col. 6, Lines 10-11)

(cl. 30) an array of conductive elements includes forming an array of solder columns (306; Col. 5, Line 53);

(cl. 31) an array of conductive elements includes forming an array of solder balls (306; Fig. 3c);

(cl. 32) applying the adhesive as a thin coating (Fig. 3a) and therefore a film; either forming an adhesive over conductors (Fig. 1a-f) forming conductors in holes of an adhesive (3a-c) by chemical etching (Col.6, Lines 10-11) and filling the holes with a paste (Col. 6, Line 12) to form the same structure (compare 1f, 3c);

(cl. 60, 61) use of solder paste (Col. 5, Lines 50-53) and therefore use of a dispensing apparatus to place paste in openings (Col. 2, Lines 19-21);

(cl. 65) the adhesive includes bevels (e.g. depression an adhesive; Fig. 3C) and therefore chamfers.

10. Nguyen'881 is silent as to how its adhesive is applied and does not explicitly disclose use of a fluid.

11. However, Nguyen'595 utilizes applying an adhesive/ encapsulant/ underfill in a state capable of flowing and therefore a fluid ("injected"; Col. 3, Lines 36-40).

12. It would have been obvious to one of ordinary skill in the art to incorporate the coating process of Nguyen'595 on the wafer of Nguyen'881 in order to provide the adhesive material on the wafer as required by Nguyen' 881 (Step 404; Fig. 4).

13. With respect to the sequence of claim 62, the prior art discloses all of the steps as the claimed method except that its sequence involved curing after the openings in an adhesive are filled with conductive material in contrast to the claimed sequence of curing an adhesive prior to filling openings. As such, since applicant has not disclosed any new or unexpected results, the step of curing prior to filling would have been obvious, since it has been held that the selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). See also Ex parte Rubin, 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).



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14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable Nguyen et al. (U.S. 6,352,881) in combination with Nguyen'595 (U.S. 6,245,595) as applied to claim 4 and further in combination with Kim et al. (U.S. 6,903,451).

15. Nguyen does not appear to show applying a protective coating to a second side of the wafer.

16. However, Kim (Fig. 24) utilizes applying a protective coating (82) to a second side (e.g., bottom) of the wafer.

17. It would have been obvious to one of ordinary skill in the art to incorporate applying a protective coating to a second side of the modified wafer including Nguyen in order to protect wafer and eliminate defects as taught by Kim (Col. 6, Lines 25-35).

18. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable Nguyen et al. (U.S. 6,352,881) in combination with Nguyen'595 (U.S. 6,245,595) as applied to claim 59 and further in combination with Yamaji et al. (U.S. 6,159,837).

19. Neither Nguyen'881 nor Nguyen'595 appears to disclose applying stencil/screen printing techniques to place paste in openings.

20. However, Yamaji utilizes applying a stencil/screen printing techniques to place paste in openings (Col. 6, Lines 3-6).

21. It would have been obvious to one of ordinary skill in the art to incorporate a screen printing process to the openings of Nguyen'881 in order to fill the openings with a conductive material as taught by Yamaji (Col. 6, Lines 3-6).

22. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable Nguyen et al. (U.S. 6,352,881) in combination with Nguyen'595 (U.S. 6,245,595) as applied to claim 59 and further in combination with Akram et al. (U.S. 6,313,522).

23. Neither Nguyen'881 nor Nguyen'595 appears to disclose that its substrate is a motherboard.

24. However, Raiser utilizes a motherboard (Col. 10, Lines 14-19).

25. It would have been obvious to one of ordinary skill in the art to form the substrate of Nguyen'881 as a motherboard in order to provide interface with external circuitry as taught by Akram (Col. 10, Lines 14-19).

#### ***Response to Amendment***

26. Applicant's arguments with respect to claims have been considered. The arguments regarding claims 1, 27, 28 and 30-33 drawn to Nguyen'595 are found unpersuasive, while applicant's remarks regarding the remaining claims are moot in view of the new ground(s) of rejection.

27. In an effort to expedite prosecution, examiner has addressed some limitations that may still be relevant.

28. First, applicant contends that Nguyen '595 does not anticipate the claimed invention, because it does not disclose forming conductive elements within an adhesive. Examiner respectfully disagrees. While applicant may have intended claim to impart a particular order to mean forming the adhesive layer first and then forming conductive elements within holes in the adhesive layer, this is not claimed as further evidenced by

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applicant's claim 3. An order is imparted by claiming it to be in the order written or presented.

29. Based on the plain and ordinary meaning of the claim, no particular order has been specified in claims 1, 27, 28 and 30-33, because whether the adhesive is formed prior or after the formations of conductive elements, the conductive elements are still formed within the adhesive. E.g. Altiris Inc. v. Symantec Corp., 318 F.3d 1363, 1371, 65 USPQ2d 1865, 1869-70 (Fed. Cir. 2003) (it was improper to read a specific order of steps into method claims where, as a matter of logic or grammar, the language of the method claims did not impose a specific order on the performance of the method steps). See also M.P.E.P 2111.01[R-5].

30. Secondly, applicant contends that the use of Nguyen'881 as a teaching reference was improper, because allegedly the proposed modification would destroy Nguyen'595 claimed invention. Although applicant's contention relied on mere conjecture that could not alone overcome examiner's prima facie case, upon further review of the case law and the claimed method of Nguyen'595, examiner agrees that a change in Nguyen'595s process as previously suggested would destroy its claimed method. However in contrast to the combination of Nguen'595 in view of Nguyen'881 as suggested in the last office action, there would be no such destruction in the new combination, supra, of Nguyen'881 in view of Nguyen'595, since Nguyen'881 is silent as to how its adhesive is applied; thus, its disclosure encompasses all known methods to apply its adhesive.

31. Lastly, with respect to applicant's statement that he reserved the right to swear behind the prior art, because applicant has not submitted an affidavit or declaration

under 37 C.F.R 1.131 that satisfied the requirements set forth in M.P.E.P 715.07[R-3], the issue is moot until properly presented.

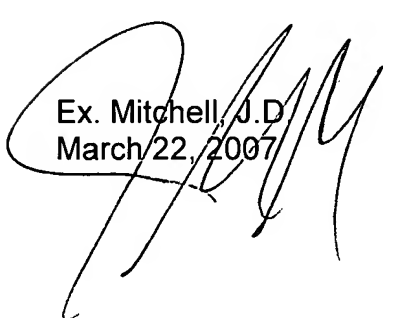
### ***Conclusion***

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses in: Buchwalter et al. (U.S. 2002/0109228), Elenius et al. (U.S. 6,441,487), Kim et al. (U.S. 6,187,615) and Yamamoto et al. (U.S. 2005/0173809) a wafer level packaging method including forming an adhesive/ resin over a wafer, forming holes in the adhesive and then filling the hole with conductive material; Raiser et al. (U.S. 6,049,124) the use of a motherboard as a substrate; and in Nozawa (U.S. 6,181,010) and Kwon et al. (U.S. 2002/0022301) the use of either a stencil or screen print to fill openings with conductive material.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Ex. Mitchell, J.D.  
March 22, 2007